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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/625,584	07/22/2003	Lawrence S. Uzelac	10559-109002	7740

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EXAMINER

TRUJILLO, JAMES K

ART UNIT	PAPER NUMBER
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2116

DATE MAILED: 01/06/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No. 10/625,584	Applicant(s) UZELAC ET AL.	
	Examiner James K. Trujillo	Art Unit 2116	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

- 1) ☒ Responsive to communication(s) filed on 01 November 2004.
- 2a) ☐ This action is **FINAL**. 2b) ☒ This action is non-final.
- 3) ☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

- 4) ☒ Claim(s) 1-27 is/are pending in the application.
- 4a) Of the above claim(s) _____ is/are withdrawn from consideration.
- 5) ☐ Claim(s) _____ is/are allowed.
- 6) ☒ Claim(s) 1-4, 6-13, 15-23 and 25-27 is/are rejected.
- 7) ☒ Claim(s) 5, 14 and 24 is/are objected to.
- 8) ☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

- 9) ☐ The specification is objected to by the Examiner.
- 10) ☐ The drawing(s) filed on _____ is/are: a) ☐ accepted or b) ☐ objected to by the Examiner.
 Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).
 Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).
- 11) ☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

- 12) ☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
- a) ☐ All b) ☐ Some * c) ☐ None of:
1. ☐ Certified copies of the priority documents have been received.
2. ☐ Certified copies of the priority documents have been received in Application No. _____.
3. ☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).
- * See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

- | | |
|---|---|
| 1) <input checked="" type="checkbox"/> Notice of References Cited (PTO-892) | 4) <input type="checkbox"/> Interview Summary (PTO-413)
Paper No(s)/Mail Date. _____ |
| 2) <input type="checkbox"/> Notice of Draftsperson's Patent Drawing Review (PTO-948) | 5) <input type="checkbox"/> Notice of Informal Patent Application (PTO-152) |
| 3) <input checked="" type="checkbox"/> Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08)
Paper No(s)/Mail Date <u>11012004</u> . | 6) <input type="checkbox"/> Other: _____ |

DETAILED ACTION

1. The office acknowledges the receipt of the following and placed of record in the file:

Oath/Declaration dated 10/14/2003 and IDS dated 11/01/2004.

2. Claims 1-27 are presented for examination.

Claim Objections

3. Claims 12 is objected to because of the following informalities: "the associated circuit" on lines 1 and 2 of the claims should be changed to "the computing system" to prevent lack of antecedent basis. Appropriate correction is required.

Double Patenting

4. The nonstatutory double patenting rejection is based on a judicially created doctrine grounded in public policy (a policy reflected in the statute) so as to prevent the unjustified or improper timewise extension of the "right to exclude" granted by a patent and to prevent possible harassment by multiple assignees. See *In re Goodman*, 11 F.3d 1046, 29 USPQ2d 2010 (Fed. Cir. 1993); *In re Longi*, 759 F.2d 887, 225 USPQ 645 (Fed. Cir. 1985); *In re Van Ornum*, 686 F.2d 937, 214 USPQ 761 (CCPA 1982); *In re Vogel*, 422 F.2d 438, 164 USPQ 619 (CCPA 1970); and, *In re Thorington*, 418 F.2d 528, 163 USPQ 644 (CCPA 1969).

A timely filed terminal disclaimer in compliance with 37 CFR 1.321(c) may be used to overcome an actual or provisional rejection based on a nonstatutory double patenting ground provided the conflicting application or patent is shown to be commonly owned with this application. See 37 CFR 1.130(b).

Effective January 1, 1994, a registered attorney or agent of record may sign a terminal disclaimer. A terminal disclaimer signed by the assignee must fully comply with 37 CFR 3.73(b).

5. Claims 1, 2, 4, 10, 19 and 23 are rejected under the judicially created doctrine of obviousness-type double patenting as being unpatentable over claims of U.S. Patent No. 6,611,918. Although the conflicting claims are not identical, they are not patentably distinct for the following reasons.
6. As to claim 1 of the instant application is unpatentable under the judicially created doctrine of "obviousness-type" double patenting with respect to claim 1 of the parent U.S. Patent

Art Unit: 2116

No. 6,611,918. As shown below claim 1 of '918 contains every element of claim 1 of the instant application and as such anticipates claim 1 of the instant application.

Patent 6,611,918	Instant Application 10/625,584
1. A leakage prevention device for a real time clock system, comprising:	1. An apparatus comprising:
a real time clock circuit having separated first and second power supply connections, and maintaining a count indicative of real time; and	a real time clock circuit;
an associated circuit, which operates in a first mode when a power supply voltage is present and operates in a second mode when battery power is present,	an associated circuit, that operates in a first mode when a power supply voltage is present and operates in a second mode when battery power is present,
said second mode providing a biasing condition that minimizes leakage current during battery operation by changing source voltage levels for the real time clock circuit.	said second mode providing a biasing condition that <i>reduces a sub-threshold off current for the real time clock circuit</i> during battery operation by <i>adjusting</i> source voltage levels for the real time clock circuit.

The only difference between '918 and the instant application is that the instant application states "reduces a sub-threshold off current for the real time clock circuit" while '918 recites "minimizes leakage current" and the instant application recites the term "adjusting" while '918 recites the term "changing".

First, the terms adjusting and changing are synonymous and therefore do not affect the interpretation of the claim.

Patent '918 minimizes leakage current. Leakage currents are sub-threshold off currents. Therefore, in minimizing leakage current it is inherent that sub-threshold current is reduced.

7. As to claim 2, claim 2 is rejected under the judicially created doctrine of obviousness-type double patenting as being unpatentable over claim 2 of U.S. Patent 6,611,918. Although the

Art Unit: 2116

conflicting claims are not identical, they are not patentably distinct from each other. As shown below in the following table shows how the two claims are not patentably distinct.

Patent 6,611,918	Instant Application 10/625,584
2. A device as in claim 1, further comprising a device which detects the presence of the power supply voltage, and switches said bias levels responsive thereto.	2. The apparatus of claim 1, wherein the associated circuit comprises one or more switching devices between source and substrate connections of the real time clock circuit.

Specifically, '918 recites switching bias levels of the real time clock circuit using the associated circuit. Bias levels can only be controlled using source and substrate voltages. Therefore, the associated circuit must comprise one or more switching devices between source and substrate connections of the real time clock.

8. As to claim 4, claim 4 is rejected under the judicially created doctrine of obviousness-type double patenting as being unpatentable over claim 4 of U.S. Patent 6,611,918. Although the conflicting claims are not identical, they are not patentably distinct from each other. As shown below in the following table shows how the two claims are not patentably distinct.

Patent 6,611,918	Instant Application 10/625,584
4. A device as in claim 1, further comprising a bias production part, driven by said battery.	4. The apparatus of claim 1, wherein said adjusting voltage levels is performed using a battery providing the battery operation.

Specifically, '918 recites using the battery to change the biasing, which is the same battery that provides the battery operation.

9. As to claim 10, claim 10 of the instant application is unpatentable under the judicially created doctrine of "obviousness-type" double patenting with respect to claims 1 and 17 of the parent U.S. Patent No. 6,611,918. As shown below claims 1 and 17 of '918 is not identical to

Art Unit: 2116

claim 10 of the instant application but the wording is such that claim 10 of the instant application is not patentably distinct from claim 17 of '918.

Patent 6,611,918	Instant Application 10/625584
1. A leakage prevention device for a real time clock system, comprising:	10. A personal computing system comprising:
a real time clock circuit having separated first and second power supply connections, and maintaining a count indicative of real time; and	a core power source (<i>first power supply with connections</i>): core power rails coupled with the core power source (<i>connections</i>); a real time clock circuit;
an associated circuit, which operates in a first mode when a power supply voltage is present and operates in a second mode when battery power is present, said second mode providing a biasing condition that minimizes leakage current during battery operation by changing source voltage levels for the real time clock circuit.	a battery coupled with the real time clock circuit; a bias-mode circuit (<i>an associated circuit</i>) that operates in a first mode when the core power source provides power, and said second mode providing a biasing condition that reduces a sub-threshold off current for the real time clock circuit during battery operation by adjusting source voltage levels for the real time clock circuit.

And,

Patent 6,611,918	Instant Application 10/625584
17. A real time clock system, comprising:	10. A personal computing system comprising:
a real time clock circuit, having a first power supply connection; and	a core power source: core power rails coupled with the core power source; a real time clock circuit
a controlling circuit for said real time clock circuit, said controlling circuit including a connection to a power supply	
and a connection to a battery including control	a battery coupled with the real time clock circuit;
and including a control circuit which connects said real time clock to said power supply connection when said power supply is available, and connects said real time clock to a low leakage bias source to change source voltage levels for said real time clock circuit	a bias-mode circuit that operates in a first mode when the core power source provides power, and said second mode providing a biasing condition that reduces a sub-threshold off current for the real time clock circuit during battery operation by adjusting source voltage

when said power supply is not available.	levels for the real time clock circuit.
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Specifically, the core power supply of '918 is the first power supply. The connections of the core power supply are the power rails. The control circuit of '918 is interpreted to be a bias-mode circuit. The bias mode circuit of '918 has a first mode that uses its core power. Patent '918 has a second mode that reduces sub-threshold off current (connects to a low leakage bias source) during battery operation.

10. As to claim 11, claim 11 of the instant application is unpatentable under the judicially created doctrine of "obviousness-type" double patenting with respect to claim 17 of the parent U.S. Patent No. 6,611,918. As shown below claim 17 of '918 is not identical to claim 11 of the instant application but the wording is such that claim 11 of the instant application is not patentably distinct from claim 17 of '918.

Specifically, claim 17 of patent 6,611,918 recites a control circuit which connects said real time clock to said power supply connection when power supply is available, and connects said real time clock to a low leakage bias source to change the source voltage levels of the real time clock circuit when said power supply is not available. It is inherent that the computing system comprises one or more switching devices between source and substrate connections of the real time clock circuit. Specifically, '918 recites the bias sources to change source voltage levels. In order to make such a change it is necessary to have a switching device. Further source and substrate connections must be changed because those connections control bias levels.

11. Claim 13 is rejected under the judicially created doctrine of obviousness-type double patenting as being unpatentable over claim 4 of U.S. Patent No. 6,611,918. Although the conflicting claims are not identical, they are not patentably distinct for the following reasons.

Patent 6,611,918	Instant Application 10/625,584
4. A device as in claim 1, further comprising a bias production part, driven by said battery.	13. The apparatus of claim 10, wherein said adjusting voltage levels is performed using a battery providing the battery operation.

Specifically, the battery in patent '918 drives the bias production part that adjusts the voltage levels.

12. As to claim 19 of the instant application is unpatentable under the judicially created doctrine of "obviousness-type" double patenting with respect to claim 1 of the parent U.S. Patent No. 6,611,918. As shown below claim 1 of '918 contains every element of claim 19 of the instant application and as such anticipates claim 1 of the instant application.

Patent 6,611,918	Instant Application 10/625,584
1. A leakage prevention device for a real time clock system, comprising:	19. A system comprising:
a real time clock circuit having separated first and second power supply connections, and maintaining a count indicative of real time; and	a real time clock circuit for maintaining a count indicative of real time; and
an associated circuit, which operates in a first mode when a power supply voltage is present and operates in a second mode when battery power is present,	source-voltage-level adjustment means for operating the real time clock with a reduced sub-threshold off current when battery power is present, <i>and for allowing the real time clock circuit to communicate with other computing components when a regular power supply voltage is present.</i>
said second mode providing a biasing condition that minimizes leakage current during battery operation by changing source voltage levels for the real time clock circuit.	

Claim 1 of '918 recites a real time clock circuit that operates in a first mode when the power supply is present. A real time clock is responsible for maintaining time information. This time information is inherently used by other computing components. Therefore it is necessary

Art Unit: 2116

that in order for the real time clock to function the real time clock must be allowed to communication with other computing components when a regular power supply voltage is present.

13. Claim 23 is rejected under the judicially created doctrine of obviousness-type double patenting as being unpatentable over claim 11 of U.S. Patent No. 6,611,918. Although the conflicting claims are not identical, they are not patentably distinct for the following reasons. Claim 23 of the instant application is unpatentable under the judicially created doctrine of “obviousness-type” double patenting with respect to claim 11 of the parent U.S. Patent No. 6,611,918. As shown below claim 11 of ‘918 is not identical to claim 23 of the instant application but the wording is such that claim 23 of the instant application is not patentably distinct from claim 11 of ‘918.

Patent 6,611,918	Instant Application 10/625584
11. A method of operating a real time clock in a personal computer, comprising:	23. A method of operating a real time clock, the method comprising:
operating a real time clock from a power supply during a first mode of operation; and	operating a real time clock circuit from a power supply during a first mode of operation; and
operating said real time clock from a battery during a second mode of operation, said operating comprising setting a bias level which minimizes leakage current during said operating by changing source voltage level for said real time clock.	operating said real time clock circuit from a battery during a first mode of operation that reduces a sub-threshold off current for the real time clock circuit by adjusting source voltage levels for the real time clock circuit.

14. Claims 6, 15, 21, and 25 are rejected under the judicially created doctrine of obviousness-type double patenting as being unpatentable over claims described above of U.S. Patent 6,611,918 in view of Volk et al., U.S. Patent 5,543,743.

Art Unit: 2116

15. As to claim 6, patent 6,611,918 substantially recites the claims according to claim 1 as described above. Patent 6,611,918 do not recite the limitations according to claim 6.

Specifically, 6,611,918 does not recite further comprising a power supply ready signal that facilitates isolation of the real time clock circuit during transition from the second mode to the first mode.

Volk teaches a power supply ready signal (POWERGOOD signal) that facilitates isolation of the real time clock signal when the power is not stable (col. 4 line 55 through col. 10 line 5 and col. 10 lines 34-51). Specifically, Volk teaches that an RTC clock should be isolated when a main power supply is switch off. Volk would suggest to those of ordinary skill in the art that isolating the RTC would prevent errors in its tracking of time when the power is not good.

It would have been obvious to one of ordinary skill in the art, having the teachings of patent 6,611,918 and Volk before them at the time the invention was made to modify the apparatus of patent 6,611,918 to include the power supply ready signal that facilitates the isolation of the real time clock as taught by Volk during transition from the second mode to the first mode in patent 6,611,918.

One of ordinary skill in the art would be motivated to make this modification in order prevent errors in the tracking of time in the RTC in view of Volk. Specifically, during the transition between the modes in 6,611,918 the power would not be stable because supplies are being changed. One of ordinary skill upon reading Volk would realize that isolation of the RTC would prevent errors.

Art Unit: 2116

16. As to claim 15, 21 and 25, as set forth hereinabove, patent 6,611,918 substantially recites the invention as per claims 10, 19 and 23 respectively. Claims 15, 21 and 25 are further rejected for the same reasons in the rejection of claim 6.

17. Claims 9, 18, 22 and 27 are rejected under the judicially created doctrine of obviousness-type double patenting as being unpatentable over claim described above of U.S. Patent 6,611,918 in view of Patwa et al., U.S. Patent 5,883,423.

18. As to claim 9, patent 6,611,918 substantially recited the claimed invention according to claim 1, as described above. The claims in '918 do not recite further comprising decoupling capacitors that inhibit switching induced errors during transition between first and second modes.

Patwa teaches using decoupling capacitors that inhibit induced errors during transition between modes (when a circuit transitions from one state to another, col. 2 lines 23-39). Patwa uses decoupling capacitors to reduce noise.

It would have been obvious to one of ordinary skill in the art, having the teachings of '918 and Patwa before them at the time the invention was made, to modify "918 to include decoupling capacitors as taught by Patwa to inhibit switching induced errors during transition between the first and second modes of '918.

One of ordinary skill in the art would be motivated to make the modification in order to reduce noise during transition between modes in '918 in view of Patwa.

19. As to claims 18, 22 and 27, they are rejected for the same reasons as claim 9.

Art Unit: 2116

20. Claims 7, 8, 16, 17 and 26 are rejected under the judicially created doctrine of obviousness-type double patenting as being unpatentable over claims described above of U.S. Patent 6,611,918 and Volk in view of Kwon et al., U.S. Patent 5,886,550.

21. As to claim 7, '918 together with Volk taught the apparatus according to claim 6 as described above. '918 does not recite and Volk do not disclose further comprising a delay element that delays the transition for the second mode to the first mode when transitioning back to use of the power supply voltage.

Kwon teaches a delay element that delays the transition from a second mode to a first mode (from off to on, col. 1 lines 5-19, col. 1 lines 40-43 and col. 2 lines 55-60). Kwon teaches that the delay circuit achieves the desired result of allowing the supply to be stable before being applied to a circuit (col. 3 lines 42-48).

It would have been obvious to one of ordinary skill in the art, having the teachings of '918, Volk and Kwon at the time the invention was made, to modify '918 to include the delay element as taught by Kwon to obtain a delay in the transition from the second mode to a first mode in '918.

One of ordinary skill in the art would be motivated to make the modification in order to ensure a stable voltage is provided to the circuit when a power supply is powered on.

22. As to claim 8, '918 together with Volk and Kwon taught the apparatus according to claim 7 above. Kwon further teaches wherein the delay element comprises a capacitor (col. 2 line 56).

23. As to claims 16, 17, and 26 they are rejected for the same reasons as in the rejection of claim 7.

Art Unit: 2116

24. Claims 3, 12 and 20 are rejected under the judicially created doctrine of obviousness-type double patenting as being unpatentable over claims described above of U.S. Patent 6,611,918.

25. As to claim 3, '918 substantially recites the apparatus according to claim 2, as described above. '918 recites switching a bias level as per claim 2 which is interpreted as one or more switching devices comprise level shifting logic. '918 does not recite one or more multiplexers.

The examiner takes official notice that multiplexers are well known in the art and are used to select one of a plurality of signals and place the selected signal on a single output line. Multiplexers are a reliable means for selecting one of a plurality of signals with desired control. Multiplexers are easily implemented and use a single output the number signal lines required is reduced.

It would have been obvious to one of ordinary skill in the art, having the patent '918 and the knowledge of the multiplexer before them, to modify the patent '918 to include multiplexers as is known to those of ordinary skill in the art to obtain switching levels.

One of ordinary skill in the art would have been motivated to make the modification because multiplexers are easily implemented, have desired control, and reduce the number of signal lines in a circuit.

26. As to claims 12 and 20, they are rejected for the same reasons as in the rejection of claim 3.

Allowable Subject Matter

27. Claims 5, 14 and 24 are objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

Art Unit: 2116

28. The following is a statement of reasons for the indication of allowable subject matter.

The prior art of record does not teach or suggest either individually or in combination resistors placed across a battery to form bias levels for the biasing condition, wherein the resistors are isolated from the battery during non-batter operation.

Conclusion

29. Any inquiry concerning this communication or earlier communications from the examiner should be directed to James K. Trujillo whose telephone number is (571) 272-3677.

The examiner can normally be reached on M-F (7:30 am - 5:00 pm) First Friday Off.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Lynne Browne can be reached on (571) 272-3670. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see <http://pair-direct.uspto.gov>. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

James Trujillo
December 29, 2004


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